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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/305,240	SHIM ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-26* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7 and 9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5-7 and 9-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the specification for a line width of the first surface region being equal to a line width of the impurity implantation region, as recited in claim 5.

Claim 10 recites a first sector not reaching either one of the source region and the drain region, wherein the impurity implantation region occupies the entire top surface of the substrate. The embodiment of figure 7 describes a first sector not reaching either one of the source region and the drain region, wherein the embodiments of figures 5 and 6 describe an impurity implantation region occupies the entire top surface of the substrate. There is no support in the specification for a device comprising a first sector not reaching either one of the source region and the drain region, wherein the impurity implantation region occupies the entire top surface of the substrate, as recited in claims 10 and 14.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

1. Claims 5-9, 11 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Although the specification recites line widths of active regions, impurity implantation regions, wherein the line widths of the active regions and the gates are defined as F and W3, respectively, it is unclear what distance is represented by the line widths of the first surface, the impurity implantation region and the first sector, as recited in claims 5, 6, 11 and 15,

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 5-7 and 9-17, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. (5,668,021) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 5, 10 and 14, Subramanian et al. teach in figure 7 and related text a transistor comprising: a semiconductor substrate 10 of a first conductivity type; source and drain regions 28, 30, 34. 36 of a second conductivity type formed in the substrate and defining between them a channel region,

an impurity implantation region 24 of impurities of a second conductivity type (column 3, lines 56-58) formed in the channel region, the impurity implantation region 24 separated from the source region and the drain region 28, 30, 34. 36, the impurity implantation region comprising a depletion channel of the second conductivity type and including a first surface of the semiconductor substrate,

an enhancement channel of the first conductivity type with uniform doping concentration and occupying a second surface of the semiconductor substrate,

a gate insulating layer 12 on the substrate over at least a portion of the first surface and the second surface, and

a gate 46 (14, 26 and 38, see column 5, lines 57-60) on the gate insulating layer over at least a portion of the depletion channel and over at least a portion of the enhancement channel..

Although Subramanian et al. do not state that the second surface of the semiconductor substrate comprises a uniform doping concentration, the embodiment of figure 7 does not recite any additional channel doping in the second surface and no special substrate doping. Note that the second surface is part of the substrate. Thus, the doping concentration of the substrate 10 is uniform, as claimed.

Subramanian et al. do not teach using the transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, and does not state that the impurity implantation region of the first sector is operable as a depletion channel, and the second sector of the channel region is operable as an enhancement channel, wherein a line width of the first surface region is equal to a line width of the impurity implantation region, and wherein the gate has a narrowest width that is greater than a line width of the impurity implantation region.

AAPA teaches in figure 1 and related text (page 2, lines 1-15) a pull up transistor B, wherein one of the source and drain regions being electrically coupled to an I/O pad 20 and the other one being electrically coupled to a Vdd terminal, wherein the gate has a narrowest width that is greater than a line width of the impurity implantation region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Subramanian et al.'s transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, and wherein a line width of the first surface region is equal to a line width of the impurity implantation region and wherein the gate has a narrowest width that is greater than a line width of the impurity implantation region, as taught by AAPA, in order to use the device in an application which requires a pull up transistor, and in order to adjust the characteristics of the device according to the requirements of the application in hand, respectively. Note that in order to operate a pull up transistor one of the source and drain regions must be

electrically coupled to an I/O pad and the other one must electrically coupled to a Vdd terminal. The combination is motivated by the teachings of AAPA who point out the need for an improved pull up transistor.

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In this case, Subramanian et al.'s transistor is capable of performing as a pull up transistor.

Regarding the claimed limitations of an impurity implantation region of the first sector being operable under field effect as a depletion channel, and the second sector of the channel region being operable under field effect as an enhancement channel, although Subramanian et al. and AAPA do not state that the impurity implantation region of the first sector is operable under field effect as a depletion channel, and the second sector of the channel region is operable under field effect as an enhancement channel, these features are inherent in Subramanian et al. and AAPA's device for the following reasons. The first sector comprises first conductive type dopants and the second sector comprises second conductive type dopants. The equivalent circuit for Subramanian et al. and AAPA's transistor is identical to the equivalent circuit for applicant=s transistor depicted in applicant's figure 7c. The equivalent circuit comprises three transistors operating at two different modes, a first sector operates at an n-channel (Subramanian

et al., column 3, lines 59-61) as a depletion transistor, and a second sector operates at a p-channel as an enhancement transistor. Therefore, while operating the transistor as a pull up transistor, the impurity implantation region of the first sector of Subramanian et al. and AAPA's transistor is operable under field effect as a depletion channel (due to the first conductive type dopants), and the second sector of the channel region is operable under field effect as an enhancement channel (due to the second conductive type dopants), as claimed.

In the alternative, regarding the claimed limitations of an impurity implantation region of the first sector being as a depletion channel, and the second sector of the channel region being as an enhancement channel, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does."(emphasis in original) Hewlett - Packard Co . v. Bausch & Lomb Inc ., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In this case, the claimed structure is not distinct from prior art's structure, because Subramanian et al. and AAPA's transistor is identical to applicant's transistor.

Regarding claim 10, Subramanian et al. teach an impurity implantation region having a lateral extent coextensive with the first sector, and occupying the entire top surface of the semiconductor substrate within the first sector.

Regarding claims 6, 11 and 15, Subramanian et al. teach in figure 7 and related text a first sector 24 having a narrower line width than a line width of the gate 46 (14, 26 and 38, see column 5, lines 57-60).

Regarding claims 7, 12 and 16, Subramanian et al. teach in figure 7 and related text a gate 46 (14, 26 and 38, see column 5, lines 57-60) comprises a first portion over the first sector and a second portion over the second sector; and the first portion is in a predetermined ratio with respect to the second portion.

Regarding claims 9, 13 and 17, Subramanian et al. teach in figure 7 and related text a first sector separated from the source region and from the drain region by substantially equal distances (column 2, lines 45-47).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hayakawa et al. (6,184,559).

AAPA teaches in figures 1-4 and related text 18. (New) An input and output terminal structure of a semiconductor device, comprising:

a Vdd terminal;

an I/0 pad;

an open drain transistor A with a source region and a drain region defining between them a channel region, and a gate having a length, one of the source region and the drain region being electrically coupled to the Vdd terminal, the other one of the source region and the drain region being grounded; and

an enhancement transistor B with a gate having a length and with a source region and a drain region defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/0 pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal.

AAPA does not teach an enhancement transistor with a gate having a length that is greater than a length of the gate of the open drain transistor.

Hayakawa et al. teach in figure 1 an enhancement transistor with a gate having a length that is greater than a length of the gate of the open drain transistor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an enhancement transistor with a gate having a length that is greater than a length of the gate of the open drain transistor in AAPA's device in order to improve and adjust the characteristics of the device according to the requirements of the application in hand.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Hayakawa et al., as applied to claim 18 above, and further in view of Subramanian et al.

Regarding claim 19, AAPA and Hayakawa et al. teach substantially the entire claimed structure, as applied to claim 18 above, except an impurity implantation region having impurities of the second conductivity type that is formed in the channel region, that is separated from the source region and the drain region, and that includes a first surface of the semiconductor substrate, the impurity implantation region configured to function as a depletion channel.

Subramanian et al. teach in figure 7 and related text a an enhancement transistor comprises: a semiconductor substrate of a first conductivity type, wherein the source region and the drain region are of a second conductivity type and formed in the semiconductor substrate; an impurity implantation region 24 having impurities of the second conductivity type that is formed in the channel region, that is separated from the source region and the drain region, and that includes a first surface of the semiconductor substrate, the impurity implantation region configured to function as a depletion channel; an enhancement channel of the first conductivity type with uniform doping concentration, the enhancement channel including a second surface of the semiconductor substrate; and a gate insulating layer on the semiconductor substrate over at least a portion of the first surface and the second surface.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an impurity implantation region having impurities of the second conductivity type that is formed in the channel region, that is separated from the source region and the drain region, and that includes a first surface of the semiconductor substrate, the impurity implantation region configured to function as a

depletion channel in AAPA and Hayakawa et al.'s device in order to improve the characteristics of the device.

Regarding claims 20-26, prior art's device comprises length of the gate of the open drain transistor is equal to a length of an impurity implantation region formed in a channel region of the open drain transistor, wherein the length of the gate of the enhancement transistor is greater than a length of an impurity implantation region formed in a channel region of the enhancement transistor, wherein one of the source region and the drain region of the open drain transistor is electrically coupled to one of the source region and the drain region of the enhancement transistor, and the other one of the source region and the drain region of the open drain transistor is grounded, wherein one of the source region and the drain region of the enhancement transistor is electrically coupled to one of the source region and the drain region of the open drain transistor, and the other one of the source region and the drain region of the enhancement transistor is electrically coupled to the Vdd terminal, wherein the impurity implantation region is separated from the source and drain regions by substantially equal distance.

Response to Arguments

Applicant argues that Subramanian et al. and APA do not teach a line width of the first surface region being equal to a line width of the impurity implantation region, as

recited in claim 5, and an impurity implantation region occupies the entire top surface of the substrate, as recited in claims 10 and 14.

There is no support in the specification for a line width of the first surface region being equal to a line width of the impurity implantation region, as recited in claim 5, and there is no support in the specification for a device comprising a first sector not reaching either one of the source region and the drain region, wherein the impurity implantation region occupies the entire top surface of the substrate, as recited in claims 10 and 14.

Applicant argues that there is support on page 11, lines 3-5 of the specification for an open drain transistor and an enhancement transistor, wherein the gate of the enhancement transistor having a length greater than the length of the gate of the open drain transistor.

The examiner did not find support on page 11, lines 3-5 of the specification for an open drain transistor and an enhancement transistor, wherein the gate of the enhancement transistor having a length greater than the length of the gate of the open drain transistor, as argued by applicant.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC

2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
March 12, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800